This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Currently Amended) The method of claim [[1]] 4, further comprising forming a passivating layer over the last metal + 1 Cu level of the Cu laminate inductor.

3. (Original) The method of claim 2, further comprising forming a passivating layer of CoWP over the last metal + 1 Cu level of the Cu laminate inductor.

4. (Currently Amended) A method of fabricating a high performance copper (Cu) laminate inductor ~~The method of claim 1, for forming a Cu inductor having an aluminum bond pad, further~~ comprising the steps of:

~~a.~~ forming a last metal layer including damascene Cu interconnects in a dielectric, one Cu interconnect including a Cu laminate inductor at the last metal level;

~~b.~~ depositing one or more layers of passivation material over the last metal layer damascene Cu interconnects;

~~c.~~ patterning terminal vias in the one or more layers of passivation material corresponding to said Cu interconnects, one terminal via including a via of the Cu laminate inductor over the last metal Cu level of the Cu laminate inductor;

~~d.~~ forming a bond pad structure above one of said Cu interconnects including depositing metal for said bond ~~pads~~ pad and a barrier layer, patterning the metal for said bond ~~pads~~ pad and barrier layer, and depositing a Cu seed layer atop said bond pad and barrier layer;

~~e.~~ depositing and patterning a resist for Cu inductors, and depositing Cu to selectively form Cu in inductor regions at a last metal + 1 Cu level of the Cu laminate inductor over the via and the last metal Cu level, to form the Cu laminate inductor; and,

~~f.~~ stripping the resist, etching the Cu seed layer, and selectively depositing a passivating layer on said Cu inductors.

5. (Currently Amended) The method of claim 4, further including:

~~g. after step f,~~ coating ~~the structure of step f~~ said last metal + 1 level having said Cu inductors and bond pad structure with polyimide, and forming openings to said bond ~~pads~~ pad; and,[[.]]

~~h.~~ depositing barrier layer metallurgy, and forming solder balls.

6. (Withdrawn) The method of claim 1, for forming a Cu inductor having a Cu bond pad, further comprising the steps of:

a. forming last metal layer damascene Cu interconnects in a dielectric;

b. depositing one or more layers of passivation material over the last metal layer damascene Cu interconnects;

c. patterning terminal vias in the one or more layers of passivation material;

d. depositing a barrier layer and Cu seed layer;

e. depositing and patterning a resist for Cu inductors, and depositing Cu to selectively form Cu in inductor regions;

f. stripping the resist, etching the Cu seed layer, and selectively depositing a passivating layer on Cu inductors and terminals.

7. (Withdrawn) The method of claim 6, further including:

g. after step f, coating the structure of step f with polyimide, and forming openings to bond pads.

h. depositing barrier layer metallurgy, and forming solder balls.

8. (Withdrawn) The method of claim 1, for forming a Cu inductor having a raised Cu bond pad, further comprising the steps of:

a. forming last metal layer damascene Cu interconnects in a dielectric;

b. depositing one or more layers of passivation material over the last metal layer damascene Cu interconnects;

c. patterning terminal vias in the one or more layers of passivation material;

d. depositing a barrier layer and Cu seed layer;

e. depositing and patterning a resist for Cu inductors, terminals and interconnect wiring, and depositing Cu to selectively form Cu in unmasked regions;

f. stripping the resist, etching the Cu seed layer, and selectively depositing a passivating layer on Cu inductors, terminals and interconnect wiring.

9. (Withdrawn) The method of claim 8, further including:

g. after step f, coating the structure of step f with polyimide, and forming openings to bond pads.

h. depositing barrier layer metallurgy, and forming solder balls.

10. (Withdrawn) The method of claim 1, further including depositing a Cu seed layer before depositing and patterning resist, followed by selective deposition of Cu, comprising:

a. after a terminal via etch, depositing a barrier layer, and depositing the Cu seed layer;

b. depositing and patterning resist for inductors, terminals and interconnects, and depositing Cu by electroplating to selectively form Cu in inductor, terminal and interconnect regions;

c. stripping the resist and etching the Cu seed layer and the barrier layer.

11. (Withdrawn) The method of claim 1, further including depositing a Cu seed layer after depositing and patterning resist, followed by blanket deposition of Cu and chemical mechanical polishing, comprising:

a. after a terminal via etch, depositing a barrier layer;

b. depositing and patterning resist for inductors, terminals and interconnects, and depositing Cu seed layer;

c. depositing Cu;

d. removing excess Cu;

e. stripping the resist and etching the barrier layer.

12. (Withdrawn) The method of claim 1, further including depositing a barrier layer and Cu seed layer after depositing and patterning resist, followed by blanket deposition of a barrier layer and Cu and chemical mechanical polishing, comprising:

a. after a terminal via etch;

b. depositing and patterning resist for inductors, terminals and interconnects, depositing a barrier adhesion layer, and depositing Cu seed layer;

c. depositing Cu;

d. removing excess Cu, removing the barrier adhesion layer;

e. stripping the resist and etching the barrier layer.

13. (Withdrawn) The method of claim 1, further including selectively depositing a passivating metal.

14. (Withdrawn) The method of claim 1, further including selectively depositing a passivating dielectric.

15. (Withdrawn) The method of claim 1, further including selectively depositing a passivating metal and a passivating dielectric.

16. (Withdrawn) The method of claim 1, further including selectively depositing a passivating metal or a passivating dielectric, etching back to form spacers, deposit dielectric layer.

17. (Withdrawn) The method of claim 1, further including selectively depositing a passivating metal or a passivating dielectric, etching back to form spacers, deposit selective metal on Cu.

18. (Withdrawn) The method of claim 1, further including selectively depositing a passivating metal or a passivating dielectric, deposit selective metal on Cu, etching back to form spacers, deposit dielectric layer.